Hall Ticket Number:

Code No. : 22655

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

M.E. (E.C.E.) II-Semester Main Examinations, September-2022

VLSI Physical Design

(Embedded Systems & VLSI Design)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Define Yield ? How it related to cost of an IC?	2	1	1	3
2.	Why higher level metal layers are used for power supply rails?	2	2	1	3
3.	What is the need of dummy resistors in the physical design of an IC?	2	1	2	3
4.	Draw the comb structure capacitor and write its advantages?	2	2	2	3
5.	Write any two scalable CMOS design rules.	2	1	3	3
6.	List out the sources of fabrication errors of an IC.	2	1	3	3
7.	What is meant by dead space in the physical design?	2	1	4	3
8.	How to reduce cross talk in the IC?	2	1	4	3
9.	What is the need of algorithms in the physical design of an IC?	2	1	5	3
10.	Distinguish between sub graph and tree?	2	1	5	3
	Part-B (5×8 = 40 Marks)				
11. a)	Explain complete VLSI design cycle with suitable examples?	4	2	1	3
b)	Draw and explain the various resistors that can be realized under BJT technology?	4	3	1	3
12. a)	In detail explain how to prevent latch up effect in the CMOS process?	4	4	2	3,4
b)	Draw the layout of CMOS two input NAND gate and represent layers in it?	4	3	2	4
13. a)	Distinguish between absolute and scalable CMOS design rules?	4	2	3	3
b)	Write the rules for constructing stick diagrams and also draw the stick diagram for the given function $f = \overline{AB + CD}$	4	3	3	3

Contd... 2

Code No. : 22655

14. a)	List out the large scale physical design issues and explain any two of them by giving suitable examples?	4	4	4	3
b)	Explain Weinberger image array technique and write its merits and demerits?	4	2	4	3,4
15. a)	Explain how the shortest path algorithm helps in global and detail routing in the physical design of an IC?	4	3	5	4
b)	Explain any one spanning tree algorithm with suitable examples?	4	2	5	4
16. a)	Briefly explain the recent trends in the VLSI Physical design cycle?	4	2	1	3
b)	How to realize Poly silicon resistor in the IC and draw its structure?	4	3	2	3,4
17.	Write short notes on any ***two*** of the following:				
a)	Hierarchical stick diagrams	4	2	3	4
b)	Sliceable and Non sliceable floor planning	4	2	4	3
c)	Breadth first Vs Depth first algorithm	4	3	5	3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

*****